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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/708,936	CHASE ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 7 is objected to because of the following informalities: In line 8 of claim 7, "effect" should be changed to "affect." Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701).

Regarding claim 1, Schaefer teaches a method of processing a wafer, the method comprising the steps of (column 1, line 45 – column 2, line 18):

- providing a semiconductor wafer (**1** in Fig. 1);
- forming first and second masking layers (**25** and **24)** on the first and second oppositely-disposed surfaces of the wafer;
- etching the first and second masking layers to define first (**25**) and second (**26**) mask patterns, respectively, the first and second mask patterns exposing regions of the first and second surfaces of the wafer, the exposed regions comprising first and second exposed regions of the first wafer surface and first exposed regions of the second wafer surface, the first mask pattern masking third and fourth regions of the first, lower wafer

surface (area under masks **26** in Fig. 1) and the second mask pattern masking second regions of the second, upper surface of the wafer (area under mask **25** in Fig. 1), the fourth regions of the first wafer surface being aligned with the second regions of the second wafer surface (**25** is aligned with the rightmost layer **26** in Fig. 1);

- forming an oxide mask on the first and second exposed regions of the first and second wafer surfaces (**27** in Fig. 1), the first and second mask patterns preventing the oxide mask from forming on the third and fourth regions of the first wafer surface and the second regions of the second wafer surface;
- removing the first and second mask patterns to expose the third and fourth regions of the first wafer surface and the second regions of the second wafer surface (note removal of masking layers **25** and **26** in the fourth drawing from the top in Fig. 1);
- etching the first, second, and third surface regions of the wafer, wherein etching of the first surface regions of the wafer produces recesses (**28**) in the first surface of the wafer and etching of the second and third surface regions of the wafer produces through-holes in the wafer (**29**); and then
- removing the oxide mask to yield a wafer with multiple through-holes and recesses (only a part of the wafer is shown in Fig. 1—column 1, lines 50-52).

Schaefer et al. does not teach forming a first and second oxide layer on oppositely-disposed first and second surfaces of the wafer, and therefore also does not teach removing the regions of the first and second oxide layers that are exposed when the masking layers **25** and **26** are removed.

Moon et al. teaches a method of etching a recess in a silicon wafer using a silicon nitride masking layer to mask a localized oxidation (LOCOS) process that forms an oxide that is subsequently used to mask an etch. Before depositing the silicon nitride masking layer (**88** in Fig. 19), Moon et al. forms a silicon oxide layer on the wafer surface (**84** in Figs. 18-21, 22) and teaches that it is standard procedure to do so in a LOCOS process (column 23, lines 18-19). Moon et al. also teaches exposing the wafer by removing a portion of the silicon oxide layer beneath the silicon nitride mask after removing the silicon nitride mask (Fig. 22A shows both the silicon nitride mask and the underlying silicon oxide removed; column 24, lines 54-62) in order to use the LOCOS oxide as a mask to etch the wafer.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Schaefer et al. and Moon et al. by using the method to process a wafer using a LOCOS oxide to mask an etch that produces a recess and a through hole as taught by Schaefer et al. and further growing an oxide layer beneath the silicon nitride masking layer and later removing this oxide layer in the regions beneath the masking pattern, as taught by Moon et al., to arrive at the invention as claimed in claim 1. The motivation for doing so at the time of the

invention would have been that it is standard procedure to do so in a LOCOS process, as expressly taught by Moon et al.

The phrase "processing a cap wafer configured for mating with a device wafer in the production of a die package" has not been given patentable weight since it only appears in the claim preamble, and none of the process steps recited in the claim requires the wafer to be used in the production of a die package.

Regarding claim 2, Schaefer et al. and Moon et al. together teach the method according to claim 1. Schaefer et al. further teaches that the first and second masking layers are formed of silicon nitride (column 1, lines 52-53).

Regarding claim 6, Schaefer et al. and Moon et al. together teach the method according to claim 1. Schaefer et al. further teaches that the step of etching the first, second, and third surface regions of the wafer to produce the through-holes and the recesses is an anisotropic etch (column 2, lines 10-11).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701) as applied to claim 1 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1, 2000).

Regarding claim 3, Schaefer et al. and Moon et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). Moon et al. further teaches that the first and second oxide layers are silicon oxide layers, and Schaefer et al. and Moon et al. together further teach that the oxide mask is formed of silicon oxide grown by oxidizing the first and second exposed regions of the first oxide layer and the

second exposed region of the second oxide layer (Schaefer, column 2, lines 2-5, Fig. 1; Moon, column 23, lines 22-29; Fig. 20). Neither reference expressly teaches that the oxide is silicon dioxide.

However, Wolf et al. teaches that silicon dioxide (SiO_2) is stable at high temperatures and adheres to silicon (pg. 265, first paragraph). Also, silicon exhibits a propensity to form SiO_2 as its stable oxide (pg. 268, last paragraph).

Therefore, at the time of the invention, it would have been obvious for one of ordinary skill in the art to use the method taught by Schaefer et al. and Moon et al. together, and also taught by claim 1, and grow silicon dioxide as the first and second silicon oxide layers and the oxide masking layer, since Wolf et al. teaches that this is the form of silicon oxide that is chemically stable at high temperatures and adherent to the silicon, and is the one most likely to form in a thermal oxidation process.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701) as applied to claim 1 above, and further in view of Okojie (U.S. 6,845,664).

Regarding claims 4 and 5, Schaefer et al. and Moon et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach the step of mating the cap wafer with a device so that the recesses of the cap wafer define cavities enclosing micromachined elements on the device wafer, bonding the cap wafer to the device wafer to form a wafer stack, and then singulating die from the wafer stack to produce multiple device packages. They also do not teach that as a result of the mating step, the through-holes provide access to bond pads on the device wafer.

Okojie teaches enclosing micromachined elements of a device (sensor membrane **603** in Fig. 6) with a wafer comprising a recess (not labeled in Fig. 6; column 12, lines 19-33) and a through-hole (**412** in Fig. 6) including the steps of bonding the cap wafer to the device wafer to form a wafer stack (column 13, lines 19-37), and then singulating die from the wafer stack to produce multiple device packages (column 13, lines 38-42). As a result of the mating step, the through-holes provide access to bond pads on the device wafer (column 11, lines 31-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to create a wafer using the method taught by Schaefer et al. and Moon et al. together, and use it to encapsulate a micromachined device element as taught by Okojie. The motivation for doing so at the time of the invention would have been that MEMS encapsulation is a known use in the art for a wafer etched with a recess and a through-hole, as Okojie demonstrates.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701) as applied to claim 1 above, and further in view of applicant's admitted prior art (APA).

Regarding claim 7, Schaefer et al. and Moon et al. together teach the method according to claim 1 (note 35 U.S.C. 103(a) rejection above). They do not expressly teach that a defect is present in at least one of the first and second mask patterns prior to the step of forming the oxide mask.

However, APA teaches that in photolithographic process involving both surfaces of a wafer, such as the one taught by Schaefer et al. and Moon et al. together, the risk

of developing defects in the mask patterns is high (instant specification paragraph 0004).

Therefore, at the time of the invention, it would be obvious for one of ordinary skill in the art to use the method taught by Schaefer et al. and Moon et al. together, and also taught by claim 1, and further have defects presence in at least one of the first and second mask patterns prior to the step of forming the oxide mask, as taught is common by APA. The step of forming the oxide mask taught by Schaefer et al. and Moon et al. together would then result in oxide forming in the defect (Moon et al. teaches in column 23, lines 46-53 that the silicon nitride mask itself oxidizes itself during the LOCOS process), and the step of etching the first, second, and third surface regions of the wafer will cause the oxide in the defect to be undercut so as not to affect the sizes and shapes of the through-holes or recesses formed in the first, second, and third surface regions of the wafer, as taught to be inherent in the instant specification (paragraph 0009—the method steps recited in this paragraph are the same as those taught by Schaefer et al. and Moon et al. together, see 35 U.S.C. 103(a) rejection of claim 1 above).

Claims 8, 9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701) and Okojie (U.S. 6,845,664).

Regarding claim 8, Schaefer et al. teaches a method of producing a device, the method comprising the steps of:

- providing a semiconductor wafer (**1** in Fig. 1);

- depositing first and second masking layers (**25** and **24)** on the first and second oppositely-disposed surfaces of the wafer;
- etching the first and second masking layers to define first (**25**) and second (**26**) mask patterns, respectively, the first and second mask patterns exposing regions of the first and second surfaces of the wafer, the exposed regions comprising first and second exposed regions of the first wafer surface and first exposed regions of the second wafer surface, the first mask pattern masking third and fourth regions of the first, lower wafer surface (area under masks **26** in Fig. 1) and the second mask pattern masking second regions of the second, upper surface of the wafer (area under mask **25** in Fig. 1), the fourth regions of the first wafer surface being aligned with the second regions of the second wafer surface (**25** is aligned with the rightmost layer **26** in Fig. 1);
- growing an oxide mask on the first and second exposed regions of the first and second wafer surfaces (**27** in Fig. 1), the first and second mask patterns preventing the oxide mask from forming on the third and fourth regions of the first wafer surface and the second regions of the second wafer surface;
- removing the first and second mask patterns to expose the third and fourth regions of the first wafer surface and the second regions of the second wafer surface (note removal of masking layers **25** and **26** in the fourth drawing from the top in Fig. 1);

- etching the first, second, and third surface regions of the wafer, wherein etching of the first surface regions of the wafer produces recesses (**28**) in the first surface of the wafer and etching of the second and third surface regions of the wafer produces through-holes in the wafer (**29**); and then removing the oxide mask to yield a wafer with multiple through-holes and recesses (only a part of the wafer is shown in Fig. 1—column 1, lines 50-52); and
- removing the oxide mask to yield a wafer with multiple through-holes and recesses (Fig. 1—only a portion of the wafer is shown-- providing a semiconductor wafer (**1** in Fig. 1);
- forming first and second masking layers (**25** and **24)** on the first and second oppositely-disposed surfaces of the wafer;
- etching the first and second masking layers to define first (**25**) and second (**26**) mask patterns, respectively, the first and second mask patterns exposing regions of the first and second surfaces of the wafer, the exposed regions comprising first and second exposed regions of the first wafer surface and first exposed regions of the second wafer surface, the first mask pattern masking third and fourth regions of the first, lower wafer surface (area under masks **26** in Fig. 1) and the second mask pattern masking second regions of the second, upper surface of the wafer (area under mask **25** in Fig. 1), the fourth regions of the first wafer surface being

aligned with the second regions of the second wafer surface (**25** is aligned with the rightmost layer **26** in Fig. 1);

- forming an oxide mask on the first and second exposed regions of the first and second wafer surfaces (27 in Fig. 1), the first and second mask patterns preventing the oxide mask from forming on the third and fourth regions of the first wafer surface and the second regions of the second wafer surface
- removing the first and second mask patterns to expose the third and fourth regions of the first wafer surface and the second regions of the second wafer surface (note removal of masking layers **25** and **26** in the fourth drawing from the top in Fig. 1);
- etching the first, second, and third surface regions of the wafer, wherein etching of the first surface regions of the wafer produces recesses (**28**) in the first surface of the wafer and etching of the second and third surface regions of the wafer produces through-holes in the wafer (**29**); and then
- removing the oxide mask to yield a wafer with multiple through-holes and recesses (only a part of the wafer is shown in Fig. 1—column 1, lines 50-52).

Schaefer et al. does not teach forming a first and second oxide layer on oppositely-disposed first and second surfaces of the wafer, and therefore also does not teach removing the regions of the first and second oxide layers that are exposed when the masking layers **25** and **26** are removed. Schaefer et al. also does not teach mating

the cap wafer with a device wafer so that the recesses of the cap wafer define cavities enclosing micromachined elements on the device wafer and the through-holes provide access to bond pads on the device wafer, bonding the cap wafer to the device wafer to form a wafer stack, and then singulating die from the wafer stack to produce multiple device packages.

Moon et al. teaches a method of etching a recess in a silicon wafer using a silicon nitride masking layer to mask a localized oxidation (LOCOS) process that forms an oxide that is subsequently used to mask an etch. Before depositing the silicon nitride masking layer (**88** in Fig. 19), Moon et al. forms a silicon oxide layer on the wafer surface (**84** in Figs. 18-21, 22) and teaches that it is standard procedure to do so in a LOCOS process (column 23, lines 18-19). Moon et al. also teaches exposing the wafer by removing a portion of the silicon oxide layer beneath the silicon nitride mask after removing the silicon nitride mask (Fig. 22A shows both the silicon nitride mask and the underlying silicon oxide removed; column 24, lines 54-62) in order to use the LOCOS oxide as a mask to etch the wafer.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Schaefer et al. and Moon et al. by using the method to process a wafer using a LOCOS oxide to mask an etch that produces a recess and a through hole as taught by Schaefer et al. and further growing an oxide layer beneath the silicon nitride masking layer and later removing this oxide layer in the regions beneath the masking pattern, as taught by Moon et al., to arrive at the invention as claimed in claim 1. The motivation for doing so at the time of the

invention would have been that it is standard procedure to do so in a LOCOS process, as expressly taught by Moon et al.

Further, Okojie teaches enclosing micromachined elements of a device (sensor membrane **603** in Fig. 6) with a wafer comprising a recess (not labeled in Fig. 6; column 12, lines 19-33) and a through-hole (**412** in Fig. 6) including the steps of bonding the cap wafer to the device wafer to form a wafer stack (column 13, lines 19-37), and then singulating die from the wafer stack to produce multiple device packages (column 13, lines 38-42). As a result of the mating step, the through-holes provide access to bond pads on the device wafer (column 11, lines 31-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to create a wafer using the method taught by Schaefer et al. and Moon et al. together, and use it to encapsulate a micromachined device element as taught by Okojie. The motivation for doing so at the time of the invention would have been that MEMS encapsulation is a known use in the art for a wafer etched with a recess and a through-hole, as Okojie demonstrates. The resulting invention is a method of producing a MEMS device package as specified in claim 8.

Regarding claim 9, Schaefer et al., Moon et al., and Okojie together teach the method according to claim 8. Schaefer et al. further teaches that the first and second masking layers are formed of silicon nitride (column 1, lines 52-53).

Regarding claim 11, Schaefer et al., Moon et al., and Okojie together teach the method according to claim 8. Schaefer et al. further teaches that the step of etching the

first, second, and third surface regions of the wafer to produce the through-holes and the recesses is an anisotropic etch (column 2, lines 10-11).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701) and Okokie (U.S. 6,845,664) as applied to claim 1 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1, 2000).

Regarding claim 10, Schaefer et al., Moon et al., and Okojie together teach the method according to claim 8 (note 35 U.S.C. 103(a) rejection above). Moon et al. further teaches that the first and second oxide layers are silicon oxide layers, and Schaefer et al. and Moon et al. together further teach that the oxide mask is formed of silicon oxide grown by oxidizing the first and second exposed regions of the first oxide layer and the second exposed region of the second oxide layer (Schaefer, column 2, lines 2-5, Fig. 1; Moon, column 23, lines 22-29; Fig. 20). None of the references expressly teaches that the oxide is silicon dioxide.

However, Wolf et al. teaches that silicon dioxide (SiO_2) is stable at high temperatures and adheres to silicon (pg. 265, first paragraph). Also, silicon exhibits a propensity to form SiO_2 as its stable oxide (pg. 268, last paragraph).

Therefore, at the time of the invention, it would have been obvious for one of ordinary skill in the art to use the method taught by Schaefer et al., Moon et al., and Okojie together, and also taught by claim 8, and grow silicon dioxide as the first and second silicon oxide layers and the oxide masking layer, since Wolf et al. teaches that

this is the form of silicon oxide that is chemically stable at high temperatures and adherent to the silicon, and is the one most likely to form in a thermal oxidation process.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (U.S. 6,723,250) in view of Moon et al. (U.S. 6,913,701) and Okojie (U.S. 6,845,664) as applied to claim 8 above, and further in view of applicant's admitted prior art (APA).

Regarding claim 12, Schaefer et al., Moon et al., and Okojie together teach the method according to claim 8 (note 35 U.S.C. 103(a) rejection above). They do not expressly teach that a defect is present in at least one of the first and second mask patterns prior to the step of forming the oxide mask.

However, APA teaches that in photolithographic process involving both surfaces of a wafer, such as the one taught by Schaefer et al., Moon et al., and Okojie together, the risk of developing defects in the mask patterns is high (instant specification paragraph 0004).

Therefore, at the time of the invention, it would be obvious for one of ordinary skill in the art to use the method taught by Schaefer et al., Moon et al., and Okojie together, and also taught by claim 8, and further have defects presence in at least one of the first and second mask patterns prior to the step of forming the oxide mask, as taught is common by APA. The step of forming the oxide mask taught by Schaefer et al. and Moon et al. together would then result in oxide forming in the defect (Moon et al. teaches in column 23, lines 46-53 that the silicon nitride mask itself oxidizes itself during the LOCOS process), and the step of etching the first, second, and third surface regions

of the wafer will cause the oxide in the defect to be undercut so as not to affect the sizes and shapes of the through-holes or recesses formed in the first, second, and third surface regions of the wafer, as taught to be inherent in the instant specification (paragraph 0009—the method steps recited in this paragraph are the same as those taught by Schaefer et al. and Moon et al. together, see 35 U.S.C. 103(a) rejection of claim 8 above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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